REMARKS

Claims 1-25 remain in the application for consideration of the Examiner.

Reconsideration of the outstanding objections and rejections are respectfully requested in light of the above amendments and following remarks.

Claims 1-6, 12-15, and 18-23 were rejected under the judicially created doctrine of obviousness-type double patenting over co-pending application 09/229,945.

Concerning Claim 1, the Examiner alleges that adding a predetermined value to the filtered output when the predetermined error vent due to media noise occurs in the recovered data is inherent.

Applicants respectfully traverse this allegation and request a teaching from the application.

Concerning Claim 12, the Examiner alleges that if equalization was removed and it would be obvious to do the remaining steps without the equalizer.

Applicants respectfully traverse this allegation and request a teaching which indicates same.

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5).

A letter with a proposed drawing correction with the changes shown in red is attached to the instant amendment.

It is respectfully submitted that this obviates the objection to the drawing.

The disclosure was objected to because of informalities.

By the instant amendment, the specification has been amended to take into consideration the helpful comments of the Examiner.

It is respectfully submitted that the disclosure is free from informalities.

Claims 1-17, 19-20, and 22-25 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

This rejection is traversed in part.

Claims 2, 7-11, 16, 17, 22, 24, and 25 have been amended taking into consideration the helpful comments of the Examiner.

However, the Examiner alleges that the filtered output signal in Claim 12 has no antecedent basis. However, the Examiners attention is directed to line 21 of Claim 12 where the antecedent basis is found.

The Examiner alleges that the claims in specifications do not define ex=+-(1). The Examiner's attention is directed to page 13, line 21 et. seq. where an explanation can be found.

Next the Examiner alleges that Claims 10, 11, 16, 17, 24, and 25 are rejected because they include tables.

Applicants respectfully submit that the tables define particular values and in that sense is definite.

It is respectfully submitted that Claims 1-25 are in full compliance with 35 U.S.C. §112 and particularly point out and distinctly claims the Applicant's invention.

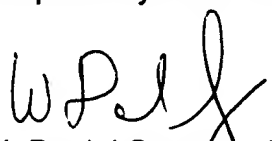
In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at line 24 of page 1 has been rewritten as follows:

In such systems, the use of EPR4 Viterbi data detection techniques is widely used. EPR4 or EFPR4 Viterbi detectors are well known, and involve probabilistic techniques for determining data states in the data channel. As data rates increase in the data channel, it becomes increasingly difficult to distinguish adjacent data pulses, and the Viterbi techniques have been found to be very useful.

Paragraph beginning at line 3 of page 2 has been rewritten as follows:

Unfortunately, significant errors still occur in data detection. For example, using EPR4 techniques, a bit error rate (BER) of about 10^{-5} typically occurs. However it has been observed that if the signal to noise ratio in a system could be ~~reduced~~ increased by, for example, only 1 dB, the bit error rate can be improved to 10^{-6}. This represents an order of magnitude improvement. Thus, even small improvements in the signal-to-noise ratio can result in large improvements in the bit error rate using EPR4 detection techniques. This is significant since presently the requirements exist for the provision of circuits that have a bit error rate less than 10^{-7}, and it is expected that this requirement will continue to become more stringent.

Paragraph beginning at line 20 of page 12 has been rewritten as follow:

The recovered write current is applied to a filter 37, which includes a series of delay elements 40 – 48 that delay the respective samples of the recovered write current at the outputs from the Viterbi 34, each for a delay time D. The delay time, D, corresponds to the sample period of the sampled data on the input line 32, and, as known, corresponds to a delay operator, equal to $e^{j\omega\square}$, where w is frequency, and □ is delay time. The filter 37 may be an FIR filter, as shown. The inputs to the delay blocks

40, 41, 43, and 44 are multiplied by weighting factors 1, 2, -2, -1, respectively, and are summed by a summer circuit 50. The output from the summer 50 is a filtered output signal derived on the output line 51.

In the claims:

Claims 1, 2, 7-11, 16, 17, 22, 24, and 25 have been amended as follows:

1. A post-processing method for correcting media noise errors and producing a ~~corrected~~ recovered data output signal, for use in a sampled data read channel of a mass data storage device that has a Viterbi detector that receives actual sampled partial response target data from a data medium of the mass data storage device, comprising:

filtering a recovered partial response target signal derived from said recovered data output signal and said sampled partial response target data to produce a filtered output signal;

providing a threshold circuit to provide a threshold against which said filtered output signal is compared;

adding a predetermined value to the filtered output signal when a predetermined error event pattern due to media noise occurs in said recovered data output signal; and modifying the recovered data output signal when said filtered output signal exceeds the threshold of said threshold circuit.

2. The method of claim 1 wherein said Viterbi detector is an ~~EPR4~~ Extended Partial Response Class 4 Viterbi detector.

7. The method of claim 1 wherein said predetermined value in an EPR4 channel is –A when said predetermined error event pattern is "1X1" where x is either 1 or 0.

8. The method of claim 1 wherein said predetermined value in an EPR4 channel is +A when said predetermined error event pattern is "0X0" where x is either 1 or 0.

9. The method of claim 1 wherein said predetermined value in an EPR4 channel is 0 when said predetermined error event pattern is other than "1X1" or "0X0" where x is either 1 or 0.

10. The method of claim 1 wherein said predetermined value in an EEPR4 channel is determined from the following tables:

Recovered Write Current (k)								Output
k	-3	-2	-1	0	1	2	3	
	X	0	0	X	0	0	X	Ajitter
	1	1	0	X	0	0	X	
	X	0	0	X	0	1	1	
	X	1	1	X	1	1	X	-Ajitter
	0	0	1	X	1	1	X	
	X	1	1	X	1	0	0	
Others								0

Polarity Check				Correction	
Amplitude	Polarity	(0)	(1)	(0)	(1)
**fexA(6) *>VthA*	*FexA(6)>0*	0	X	1	X
	FexA(6)<0	1	X	0	X
**FexB(6) *>VthA*	*FexA(6)>0*	0	1	1	0
	FexA(6)<0	1	0	0	1

wherein the polarity check correction table is logically or'd with the output of the recovered write current (k) table to produce a correction value where x is either 1 or 0.

11. The method of claim 1 wherein said predetermined value in an EPR4 channel is determined from the following table:

Recovered Write Current (k)				Output
k	-1	0	1	
	0	X	0	Ajitter
	1	X	1	-Ajitter
Others				0

and the polarity is determined from the following table:

Polarity check		Correction	
Amplitude	Polarity		
**fexA* > VthA*	*FexA > 0*	0	1
	FexA < 0	1	0

where x is either 1 or 0.

16. The method of claim 12 wherein said predetermined value in an EEPR4 channel is determined from the following tables:

Recovered Write Current (k)								Output
k	-3	-2	-1	0	1	2	3	
	X	0	0	X	0	0	X	Ajitter
	1	1	0	X	0	0	X	
	X	0	0	X	0	1	1	
	X	1	1	X	1	1	X	-Ajitter
	0	0	1	X	1	1	X	
	X	1	1	X	1	0	0	
Others								0

Polarity Check				Correction	
Amplitude	Polarity	(0)	(1)	(0)	(1)
**fexA(6) *>VthA*	*FexA(6)>0*	0	X	1	X
	FexA(6)<0	1	X	0	X
**FexB(6) *>VthA*	*FexA(6)>0*	0	1	1	0
	FexA(6)<0	1	0	0	1

wherein the polarity check correction table is logically or'd with the output of the recovered write current (k) table to produce a correction value where x is either 1 or 0.

17. The method of claim 12 wherein said predetermined value in an ~~EPR4~~ Extended Partial Response Class 4 channel is determined from the following table:

Recovered Write Current (k)				Output
k	-1	0	1	
	0	X	0	Ajitter
	1	X	1	-Ajitter
Others				0

and the polarity is determined from the following table:

Polarity check		Correction	
Amplitude	Polarity		
**fexA* > VthA*	*FexA > 0*	0	1
	FexA < 0	1	0

where x is either 1 or 0.

22. The circuit of claim 18 wherein said Viterbi detector has a partial response level of at least ~~EPR4~~ Extended Partial Response Class 4.

24. The method of claim 18 wherein said predetermined value in an EEPR4 channel is determined from the following tables:

Recovered Write Current (k)								Output
k	-3	-2	-1	0	1	2	3	
	X	0	0	X	0	0	X	Ajitter
	1	1	0	X	0	0	X	
	X	0	0	X	0	1	1	
	X	1	1	X	1	1	X	-Ajitter
	0	0	1	X	1	1	X	
	X	1	1	X	1	0	0	
Others								0

Polarity Check				Correction	
Amplitude	Polarity	(0)	(1)	(0)	(1)
**fexA(6) *>VthA*	*FexA(6)>0*	0	X	1	X
	FexA(6)<0	1	X	0	X
**FexB(6) *>VthA*	*FexA(6)>0*	0	1	1	0
	FexA(6)<0	1	0	0	1

wherein the polarity check correction table is logically or'd with the output of the recovered write current (k) table to produce a correction value where x is either 1 or 0.

25. The method of claim 18 wherein said predetermined value in an EPR4 channel is determined from the following table:

Recovered Write Current (k)				Output
k	-1	0	1	
	0	X	0	Ajitter
	1	X	1	-Ajitter
Others				0

and the polarity is determined from the following table:

Polarity check		Correction	
Amplitude	Polarity		
**fexA* > VthA*	*FexA > 0*	0	1
	FexA < 0	1	0

where x is either 1 or 0.